Abstract of the Disclosure:

In a cache memory whose addresses are split into tag, index and offset parts, a transformation device is provided in hardware form for performing a transformation between a respective tag part of the address and a coded tag address that is unambiguous in both directions. In addition, the index field of the addresses of the cache memory can be encoded by another mapping procedure that maps the index field onto a coded index field and is unambiguous in both directions. A hardware unit of suitable configuration is also used for this purpose.

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